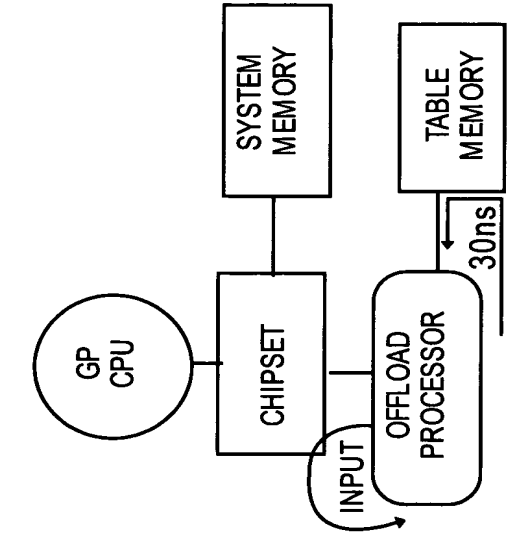




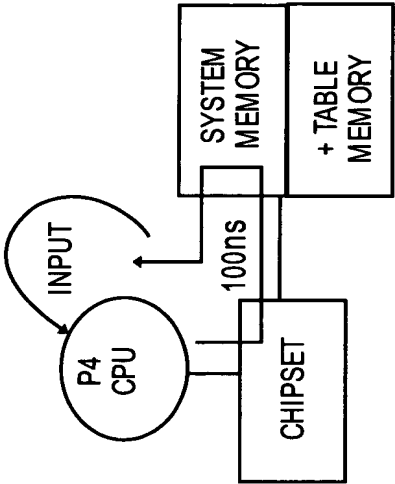
PROPERTIES OF DFA AND NFA TECHNIQUES USED ON CONVENTIONAL MICROPROCESSORS	STORAGE BOUND ON # OF STATES (FOR R CHARACTER REGULAR EXPRESSION)	EVALUATION TIME (FOR N BYTES OF INPUT) [ORDER OF]
DETERMINISTIC FINITE STATE AUTOMATA OR DFA RUNNING ON A GP CPU	2^R (NEEDS VERY LARGE MEMORY)	N MEMORY ACCESS CYCLES
NON-DETERMINISTIC FINITE STATE AUTOMATA NFA RUNNING ON A GP CPU	R	$R * N$ CPU CACHE+BRANCH CYCLES

FIG. 1A

COPROCESSOR CLOSER TO TABLE IN SRAM



CPU WALKING DFA TABLE IN DRAM

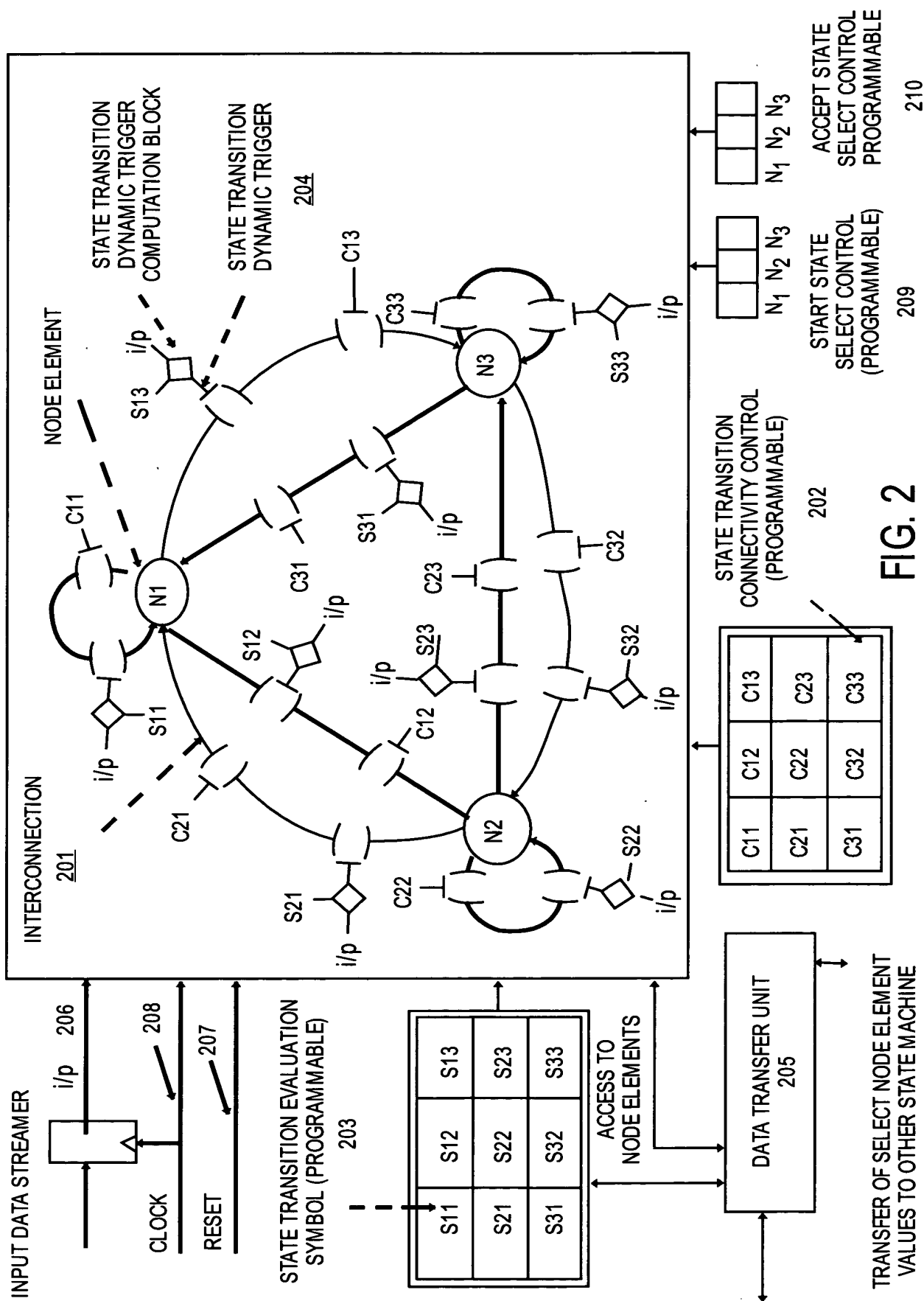


PERFORMANCE ON EVALUATING REGULAR EXPRESSIONS ON EVERY BYTE OF INPUT STREAM

1000s OF RES @ 100 Mbps
GIGABYTES OF MEMORY

100s OF RES @ 280 Mbps
100s OF MBs OF SRAM

FIG. 1B



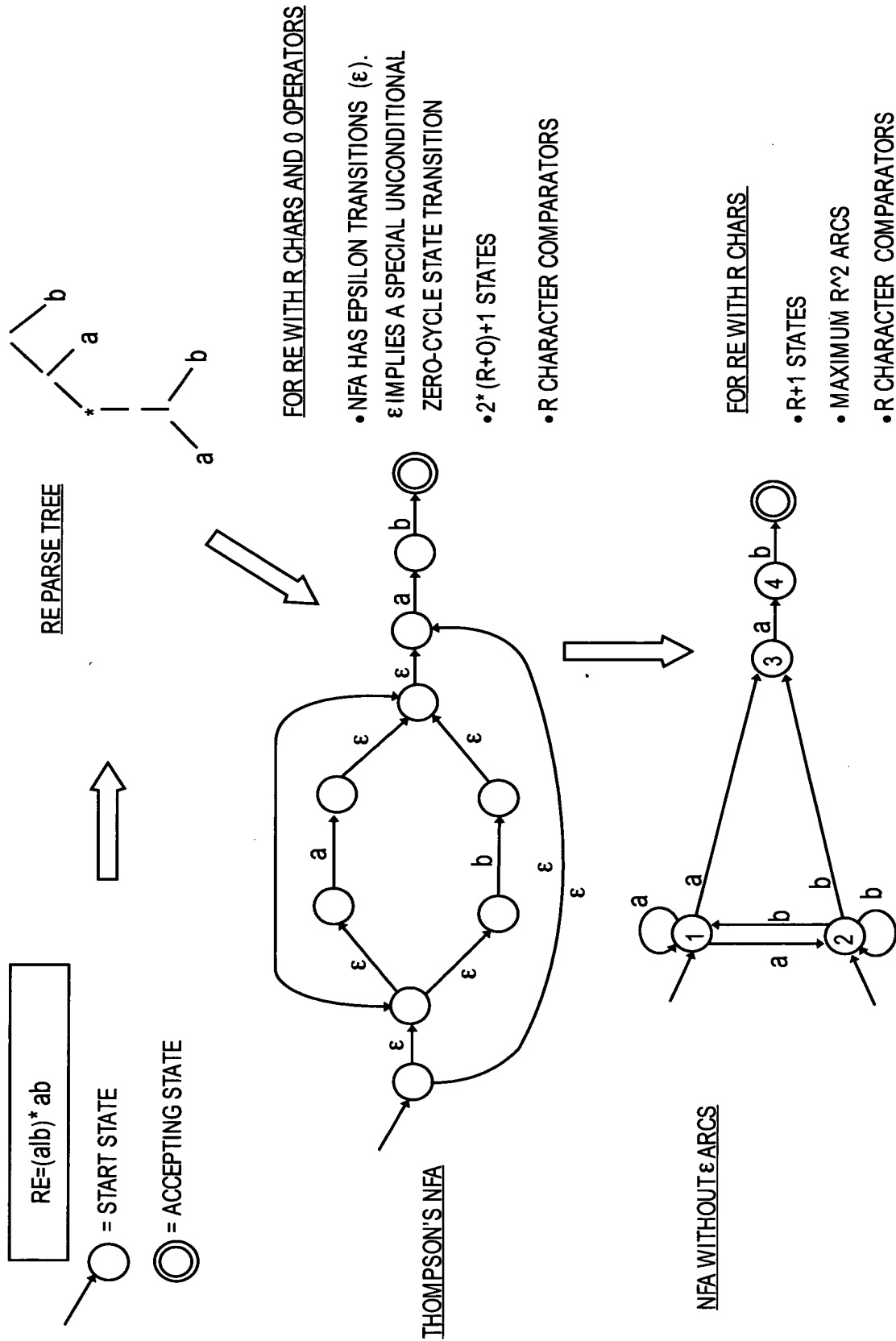
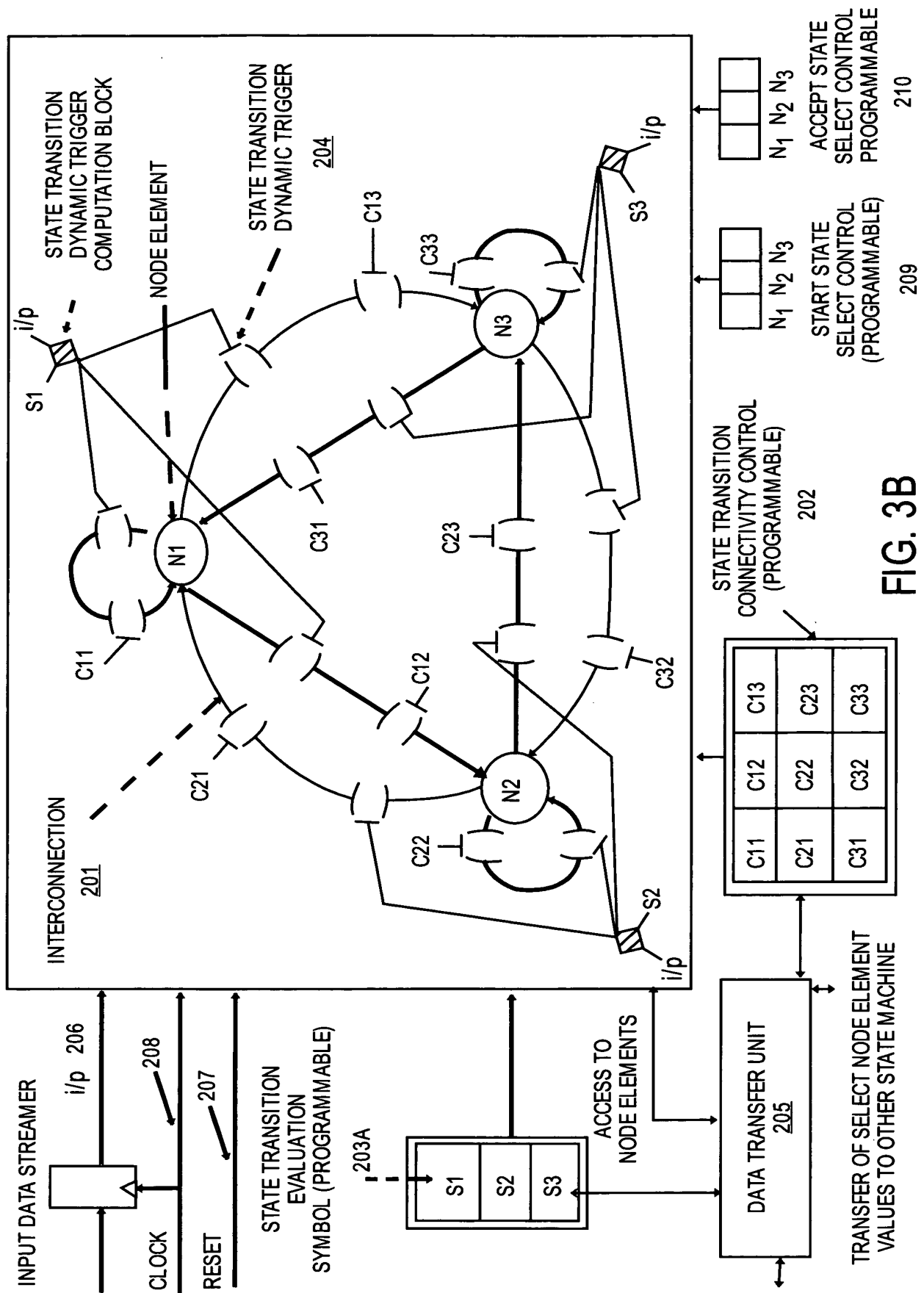


FIG. 3A



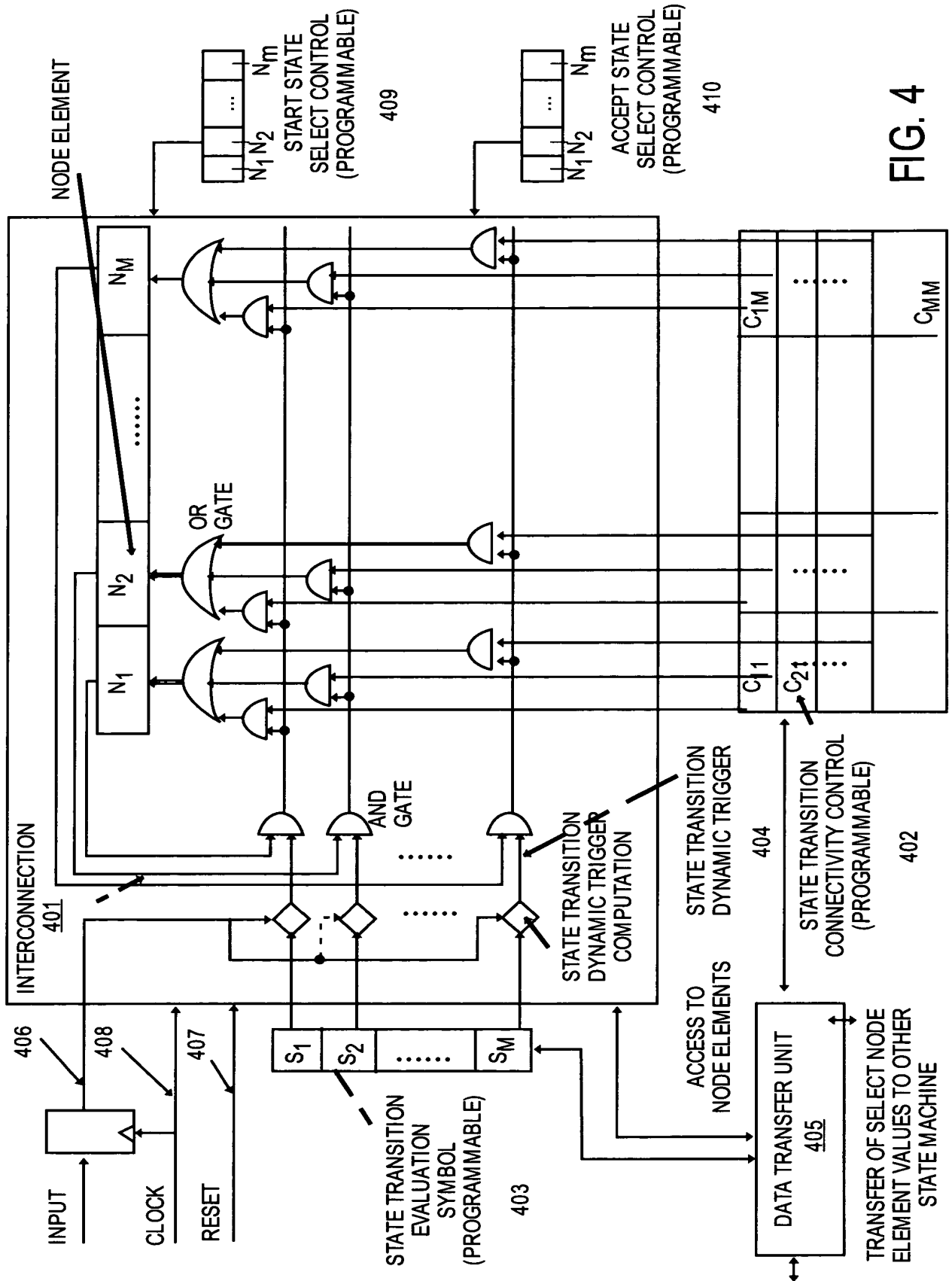


FIG. 4

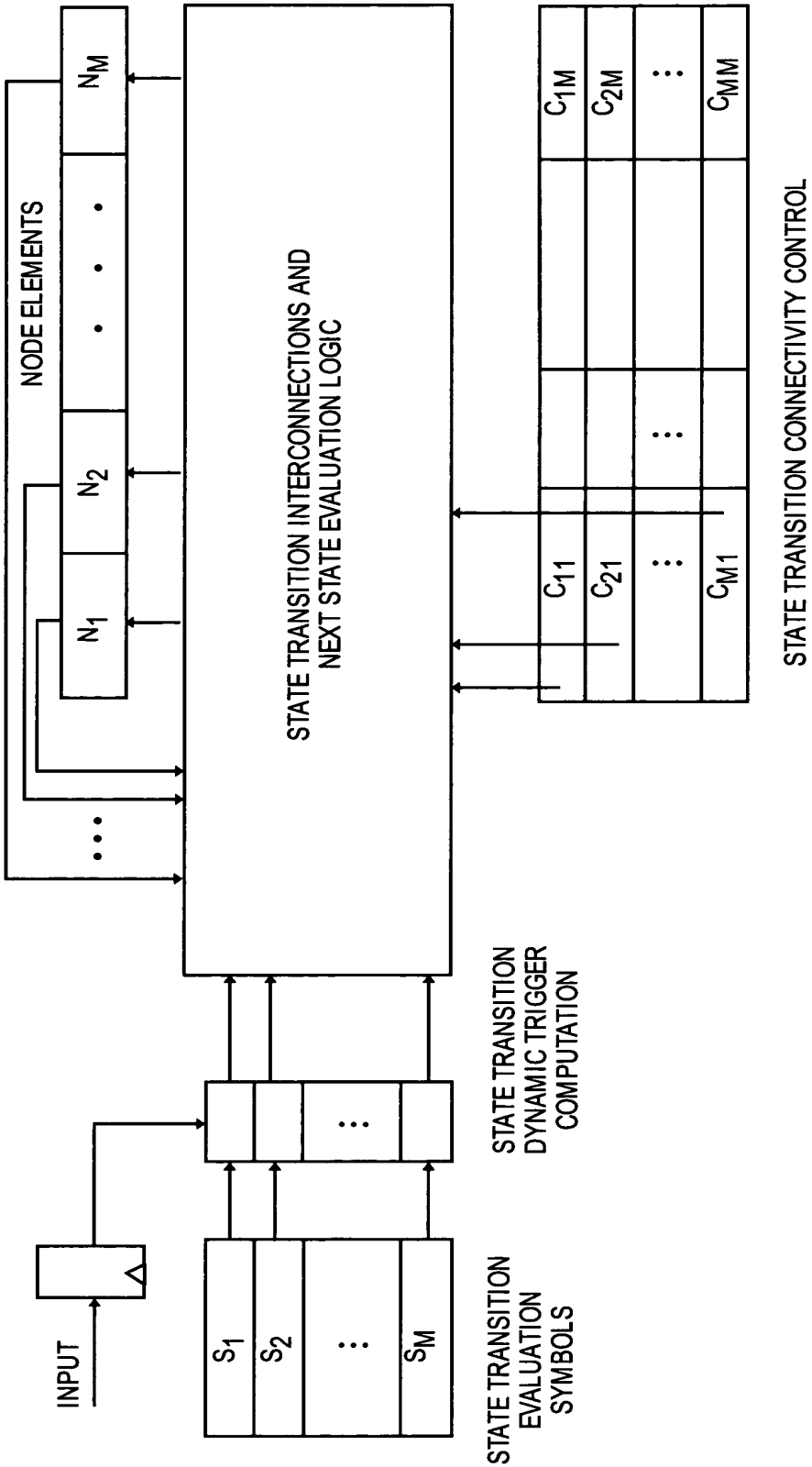
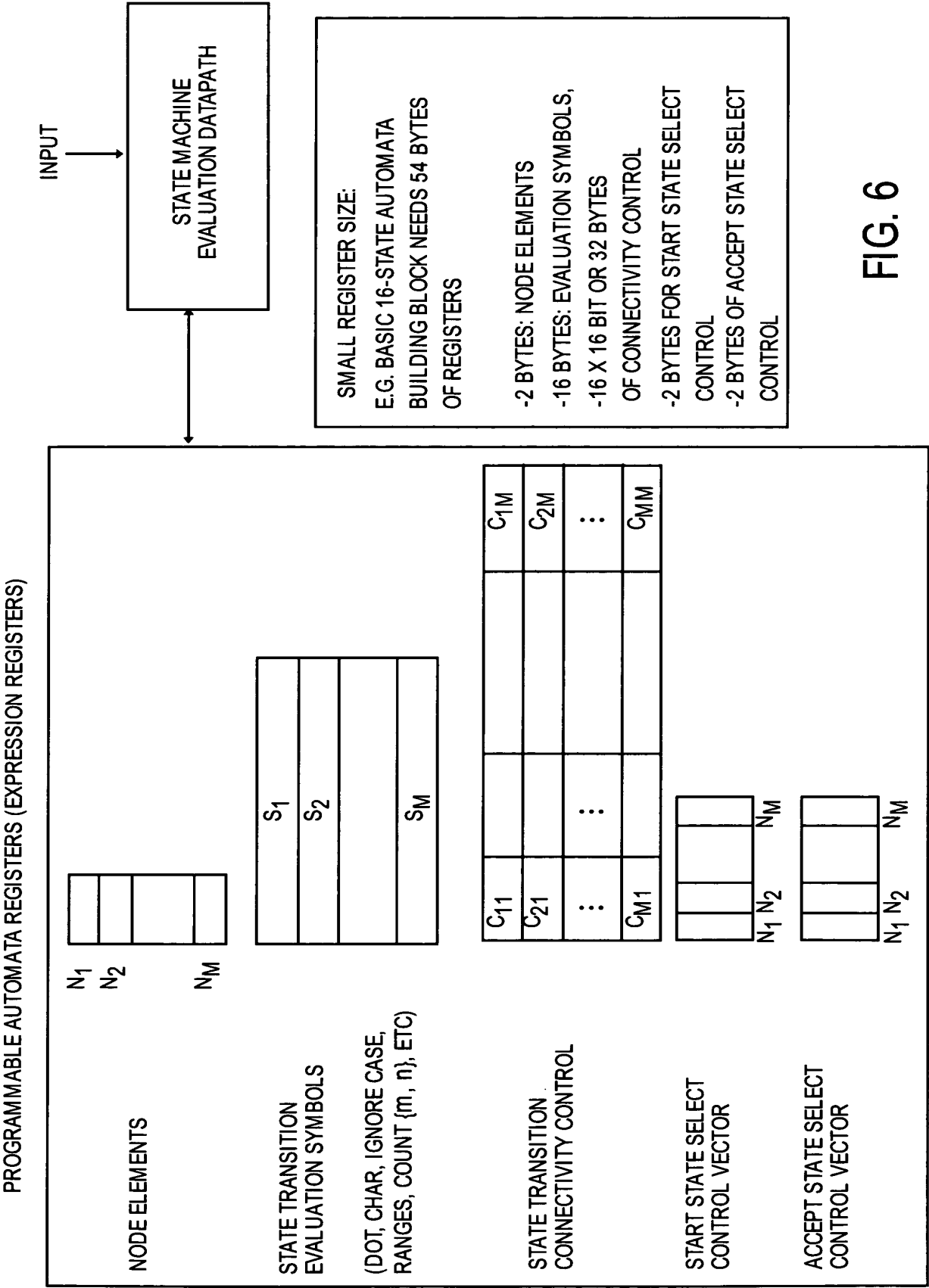


FIG. 5



- SIMPLE REGULAR STRUCTURE ENABLES A HIGH DENSITY → DENSE ARRAY OF MULTIPLE TILES
- SEVERAL THOUSANDS OF AUTOMATA (ORGANIZED AS MULTIPLE ROWS OF TILES) CAN FIT ON A SINGLE DIE ON 0.13u TECHNOLOGY

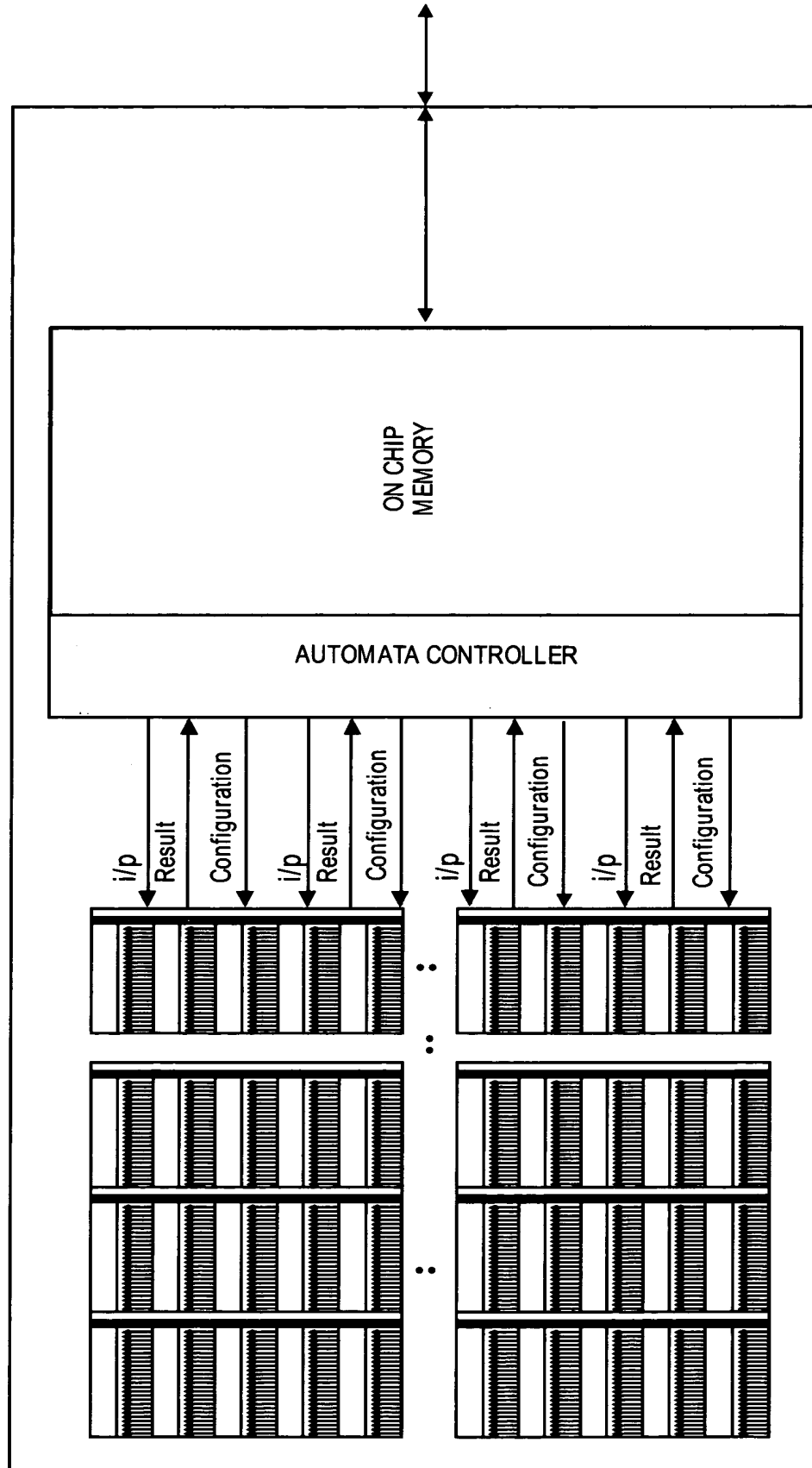
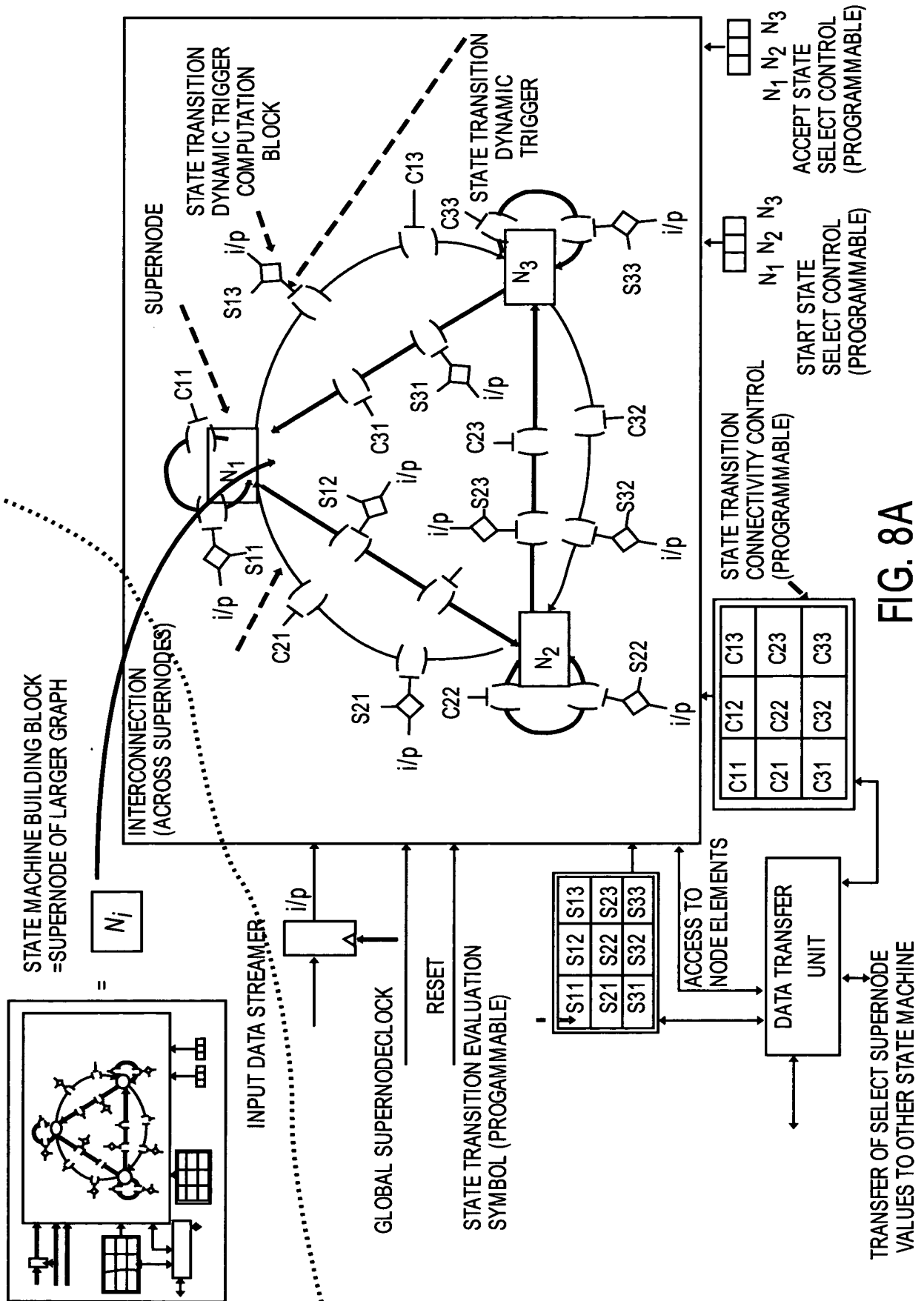


FIG. 7



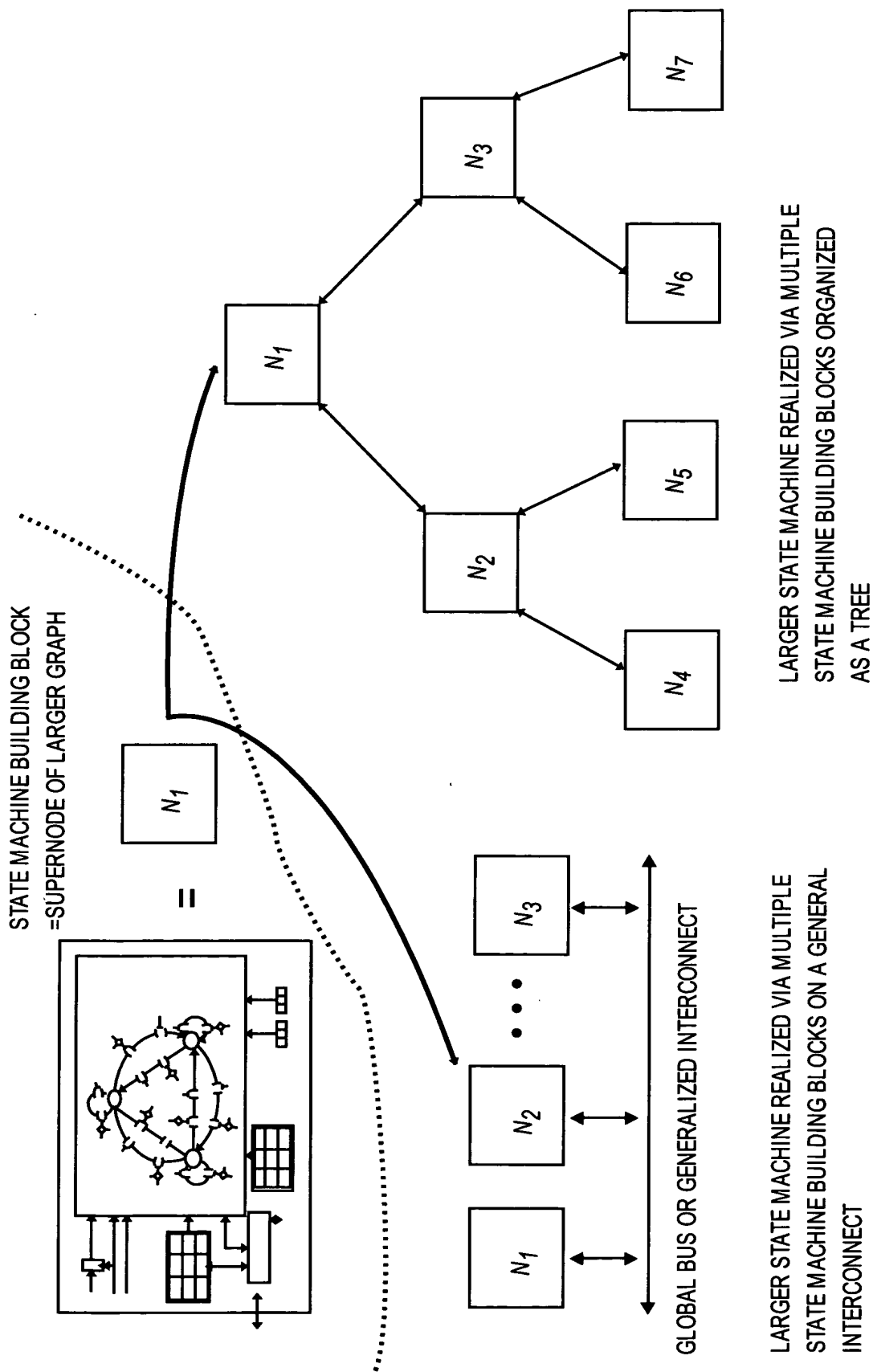


FIG. 8B


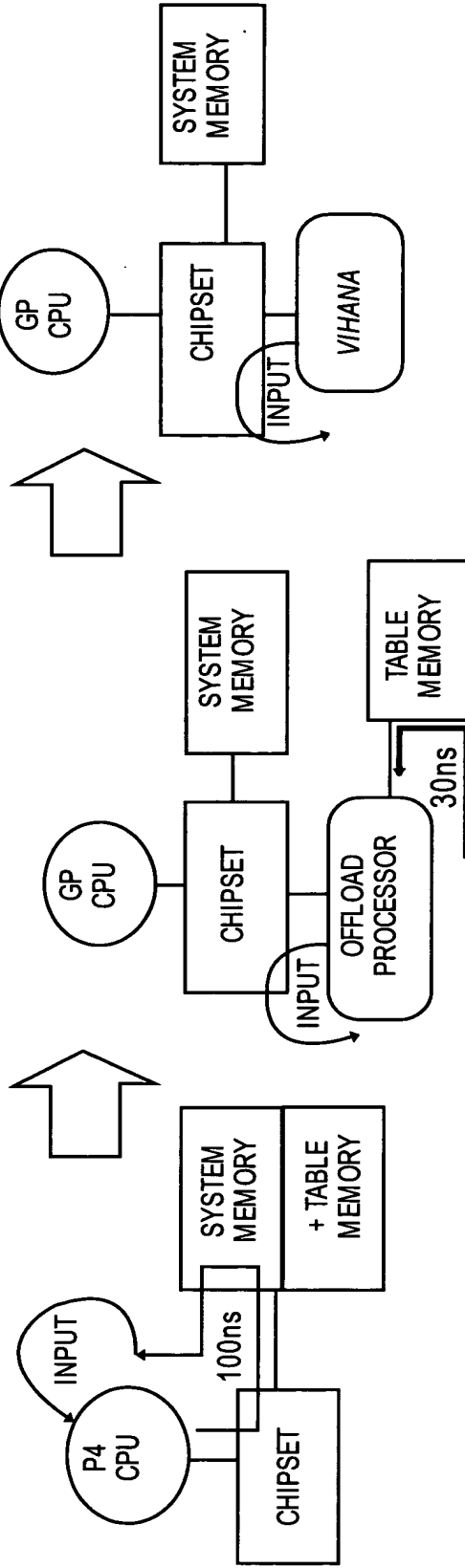
PROPERTIES OF DFA AND NFA TECHNIQUES USED ON CONVENTIONAL MICROPROCESSORS	STORAGE: BOUND ON # OF STATES (FOR R CHARACTERS)	EVALUATION TIME (FOR N BYTES) [ORDER OF]
DETERMINISTIC FINITE STATE AUTOMATA OR DFA RUNNING ON A GP CPU	2^R (NEEDS VERY LARGE MEMORY)	N MEMORY ACCESS CYCLES (~100ns)
NON-DETERMINISTIC FINITE STATE AUTOMATA OR NFA RUNNING ON A GP CPU	R	$R * N$ CPU CACHE+BRANCH CYCLES (~4ns)
		
NON-DETERMINISTIC FINITE STATE AUTOMATA OR NFA RUNNING ON THE APPARATUS	R	N TIGHT ON CHIP STATE TRANSITION CYCLE (~1 ns)

FIG. 9A
(PRIOR ART)

CPU WALKING DFA TABLE IN DRAM

COPROCESSOR CLOSER TO TABLE
IN SRAM

REGULAR EXPRESSION CO-
PROCESSOR USING EXEMPLARY STATE
MACHINE ARCHITECTURE



PERF ON RES ON EVERY BYTE

1000s OF RES @ 100 Mbps

GIGABYTES OF MEMORY

100s OF RES @ 280 Mbps

100s OF MBs OF SRAM

1000s OF RES @ > 10Gbps

NO TABLE MEMORY NEEDED

TWO ORDERS OF MAGNITUDE SPEEDUP WITHOUT NEED FOR TABLE MEMORY

FIG. 9B